REMARKS

This is in response to the Office Action of 29 June 2004. Claims 1-15, are pending in the application, and Claims 1-15 have been rejected.

By this Response, Claims 1-15 have been amended.

No new matter has been added.

In view of the amendments above and remarks below, Applicants respectfully request reconsideration and further examination.

About The Invention

The present invention relates generally to methods and apparatus for accessing memory in a secure manner from both a wired and wireless interface.

Non-narrowing Amendments

Claims 1-15 have amended in a non-narrowing manner to delete the occurrence of reference numerals therefrom.

Claims 1 and 7 have been further amended in a non-narrowing manner to replace the language "circuit parts (13, 14, 15)" with "a first voltage supply means, a first clock generator, and a first signal conversion means"; and to replace the language "circuit parts (27, 28, 29)" with "a second voltage supply means, a second clock generator, and a second signal conversion means". Support for this amendment can be found in the specification at pages 7 and 11, and in Fig. 1.

Rejections under 35 USC §102(e)

Claims 1-2, 6-8, and 12-13 have been rejected under 35 USC §102 (e) as being anticipated by Reiner, et al., (US Patent 5,875,450).

Reiner, et al., disclose a device for processing and storing data, in

particular a chip card, that includes a first interface with contacts and a second contactless interface; a first controllable switching device that is operable to selectively connect either the first interface or the second interface to a memory, through a second controllable switching device, by way of address, data, and control lines; a logic circuit that drives the first controllable switching device; the second controllable switching device disposed between the first switching device and the memory, the second controllable switching device being driven by the logic circuit and by an address signal present on the address lines. In other words, Reiner, et al., disclose a contacted interface and a contactless interface, each of which obtains address, data, and control signals from the devices to which they are respectively interfaced, and the two interfaces supply these respective address, data, and control signals to a multiplexer (i.e., first controllable switching device 3) that selects which set of address, data, and control signals are passed through to the second controllable switching device. Reiner, et al., additionally disclose a second multiplexer (i.e., second controllable switching device 7) that receives the output of the first multiplexer, and either passes these signals to the memory, or which may "interrupt connection lines between the first controllable switching device 3 and the semiconductor memory 5" (col. 4, lines 54 through col. 5, line 2).

Reiner, et al., disclose that the switching logic 4, which controls the second controllable switching device, makes its determination as to whether to allow a memory access based on the address, control, and data signals of the selected interface. There is no provision disclosed by Reiner, et al., for using the contents of the memory to be accessed in the determination of whether to permit that memory to be accessed.

Independent Claims 1, 7, and 13 have been amended to recite that access to the memory is based, at least in part, on the contents of the memory. This is different from the disclosure of Reiner, et al. Support for these amendments can be found in the specification at page 9, line 24 through page 10, line 22.

As noted above, Reiner, et al., show that access to the memory is determined without consideration of the contents of the memory to be accessed. There is no suggestion or motivation provided by Reiner, et al., to base the access to the memory, at least in part, on the contents of the memory to be accessed.

In view of the foregoing, Applicants respectfully submit that the rejection of independent Claims 1, 7 and 13, under 35 USC §102(e) have been overcome. Similarly, Applicants submit that the rejection of dependent Claims 2, 6, 8, and 12, have also been overcome.

Rejections under 35 USC §103(a)

Claims 3, 5, 9, 11, and 14-15 have been rejected under 35 USC §103(a) as being unpatentable over Reiner, et al. Claims 4 and 10 have been rejected under 35 USC 103(a) as being unpatentable over Reiner, et al., in view of Schwarz, et al., (US Patent 5,675,645).

Reference is made to Applicants' remarks above, in which an explanation is provided showing the differences between the amended independent Claims and the disclosure of Reiner, et al. More particularly, the references do not disclose, suggest, or provide motivation for the recited limitations regarding the basing of memory access at least in part upon the contents of the memory to be accessed.

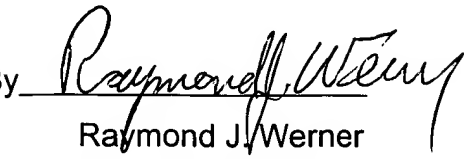
In view of the foregoing, Applicants respectfully submit that the rejection of Claims 3, 5, 9, 11, and 14-15 under 35 USC §103(a) have been overcome.

Conclusion

All of the rejections in the outstanding Office Action of 29 June 2004 have been responded to, and Applicants respectfully submit that the pending Claims 1-15 are now in condition for allowance.

Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

By 

Dated: 20 September 2004
Hillsboro, Oregon

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